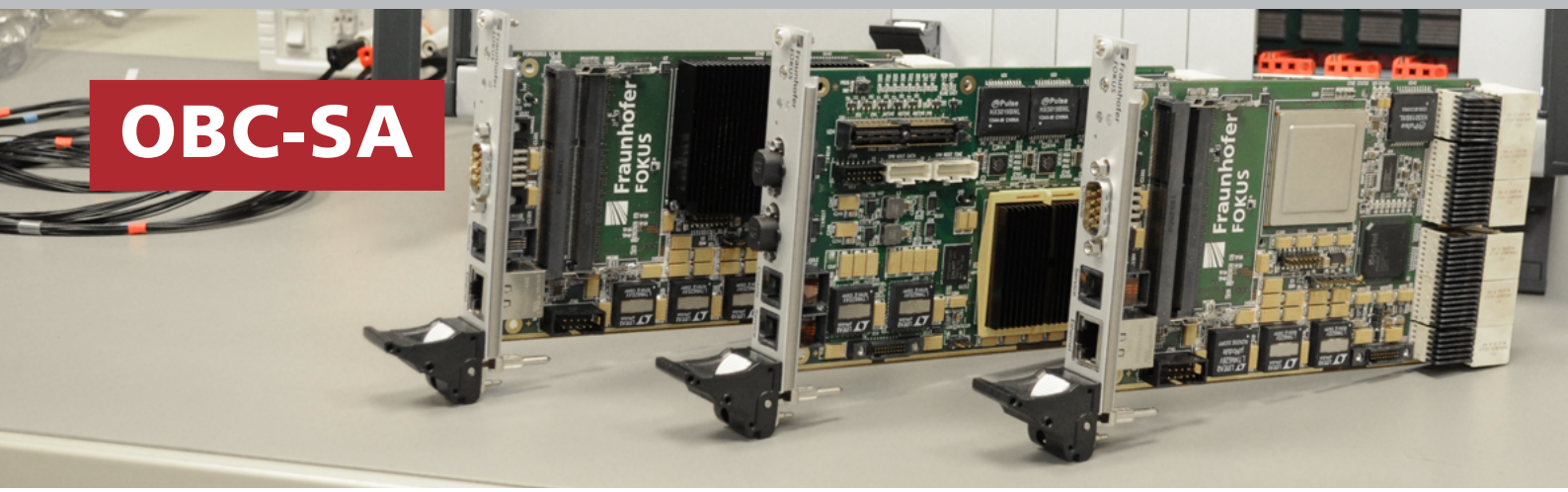
Fraunhofer FOKUS

FRAUNHOFER INSTITUTE FOR OPEN COMMUNICATION SYSTEMS FOKUS

OBC-SA



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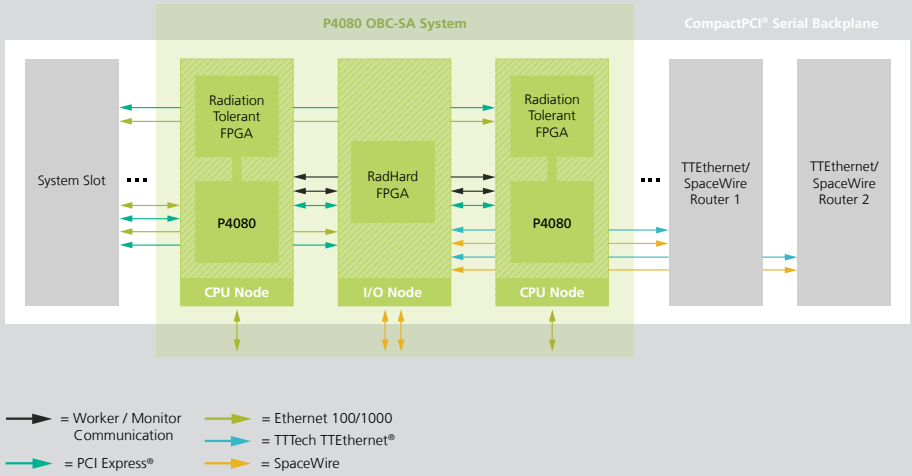
Project Partners:

Computer systems for space flight applications require ever increasing amounts of computing power to enable (on-the-fly) preprocessing of large data sets from sophisticated experiments and payloads, or even to perform realtime computation of safety-critical control commands. Without this, spacecrafts would be unable to perform complex docking maneuvers or landing approaches autonomously. Besides meeting high performance requirements, the on-board computer systems must also provide interfaces that allow their embedment in a spacecraft's often redundant communications infrastructure or support redundant ports for instruments with very high data transfer rates in the gigabit range.

On-Board Computer System Architecture

With this in mind, the On-Board Computer - System Architecture (OBC-SA) project is developing an architectural framework for future on-board computer systems to enable the modular integration of systems with different performance and functional characteristics into the IT infrastructure of a spacecraft. To this end, the project partners are developing a demonstration system consisting of two fault-tolerant on-board computers. One computer is based on the Intel Atom® processor with a triple modularity redundancy (TMR) architecture and the seconds is a dual modular redundancy (DMR) system with the high-end P4080 embedded multicore processor from Freescale. They use the PikeOS real-time operating system, which also supports the partitioning of the P4080 processor's resources. Also implemented on the basis of 1 Gbps Time-Triggered (TT) Ethernet technology is a redundant interconnect network that enables further computers and subsystems to be hooked up quickly and easily. In addition, the project is developing an I/O component that allows sensors and other low-speed I/O devices to be connected to the fault-tolerant TT Ethernet network.



Embedding the P4080 system (DMR) to the OBC-SA connection structure

The compact and robust design of the OBC-SA framework is based on the new CompactPCI® Serial industrial standard. The shared CompactPCI® Serial backplane provides communication connections for all subsystems. The OBC-SA framework and the modular design of the CompactPCI® Serial standard allow for easy configuration of future on-board computer systems from different computer and I/O components. This means that functionality, computing power, redundancy and I/O interfaces can be flexibly adapted to mission-specific requirements.

P4080 Multicore Processor

The fault-tolerant on-board computer developed by Fraunhofer FOKUS is based on the P4080, an 8-core CPU from Freescale's QorIQ PowerPC multicore family. The processor can be operated at a clock speed of up to 1.5 GHz, thus theoretically reaching a maximum speed of approximately 60 GIPS (giga instructions per second). The P4080 processor benefits from the low-power silicon-on-insulator (SOI) technology, which is also less radiation-sensitive than conventional CMOS technology. The project has validated the system's lower radiation sensitivity to the total ionizing dose (TID) and single event upsets (SEUs) in a number of irradiation tests. The SOI technology is also largely latch-up-free. Furthermore, the P4080 offers the advantages of a highly integrated embedded processor: all important functions are already integrated on-chip, which made it possible to implement an entire compute node on a single 3U cPCI® Serial board.

System Architecture

Despite the SOI technology's low radiation sensitivity, the conditions encountered in space mean that sporadic radiation-induced faults in the P4080 processor and the other COTS-based components of a compute node cannot be ruled out. In order to meet, nonetheless, the high reliability and availability requirements for space systems, effective fault tolerance mechanisms are essential at all levels of a COTS-based computer system. The P4080-based high-performance computer is configured as a dual modular redundancy (DMR) system. It consists of two identical compute nodes with a shared I/O backplane. The OBC-SA-specific interfaces were implemented with suitable IPs as part of an radiation hard FPGA on the mission specific I/O backplane.

Technology

- CompactPCI® Serial (PICMG® CPCI-S.0) peripheral slot
- P4080 8-core processor
- »QorIQ« PowerPC multicore family (Freescale)
- Clock speed: up to 1,5 GHz
- Maximum speed: approximately 60 GIPS (giga instructions per sec)
- Silicon-on-insulator (SOI) technology
- Multi-gigabit communication channels
- Flexible interface configuration through separate Xilinx Virtex-5-based I/O board
- Radiation-tolerant FPGA module with triple modularity redundancy (TMR) logic
- Synchronization and voting unit (TMR)
- SYSGO PikeOS real-time operating system
- Fast parallel processing algorithms

Funding

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